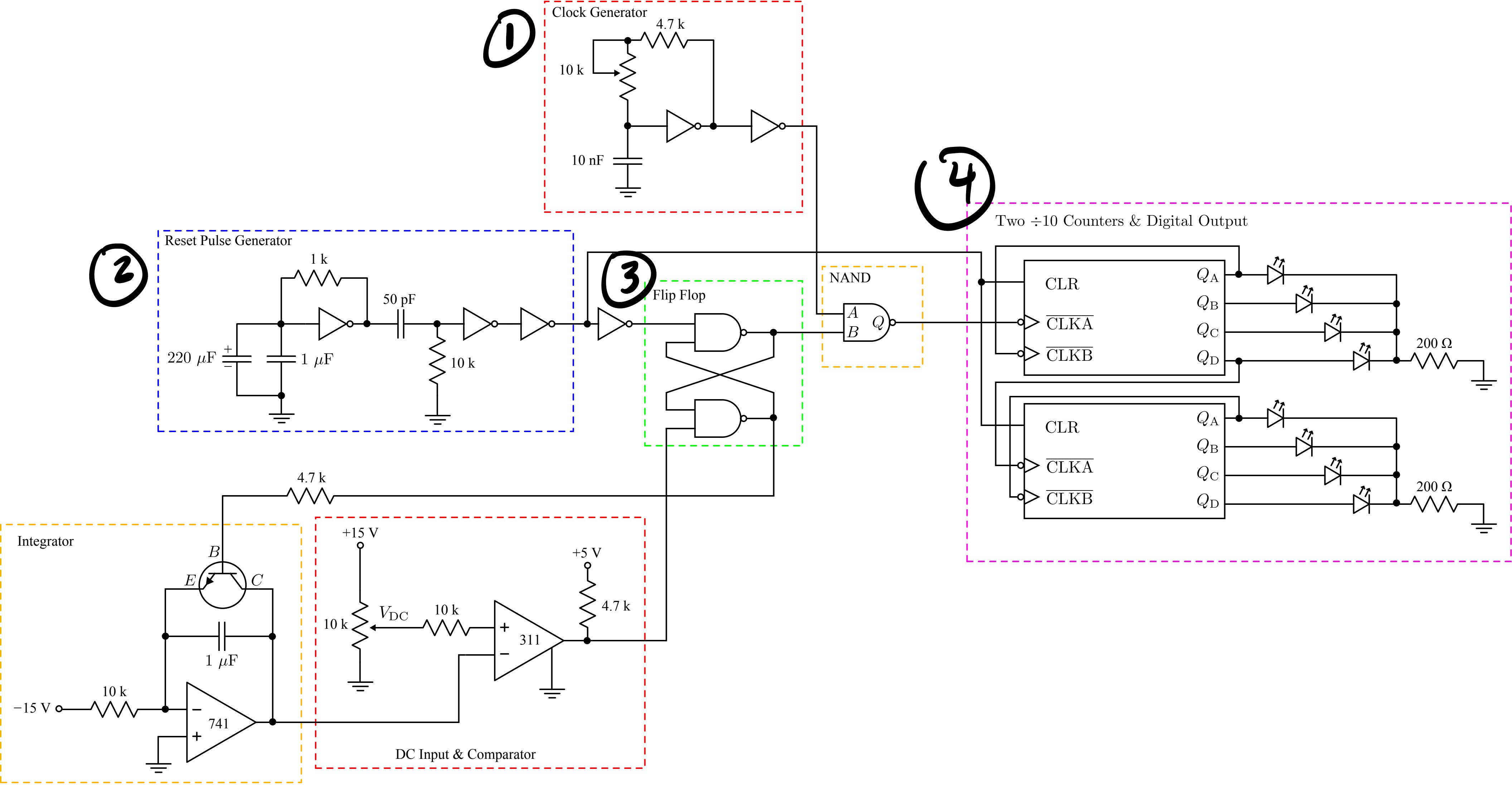


1
Clock Generator
4.7 k
10 k
10 nF
2
Reset Pulse Generator
1 k
50 pF
220 μF
1 μF
10 k
3
Flip Flop
NAND
A
B
Q
4
Two ÷10 Counters & Digital Output
CLR
CLKA
CLKB
QA
QB
QC
QD
200 Ω
CLR
CLKA
CLKB
QA
QB
QC
QD
200 Ω
4.7 k
Integrator
B
E
C
1 μF
10 k
−15 V
741
DC Input & Comparator
+15 V
10 k
VDC
10 k
311
+5 V
4.7 k

PHYS 231 - Nov. 22, 2023

Today: 1. Preview Day 1 of Analog-to-Digital Converter (ADC) final Project.

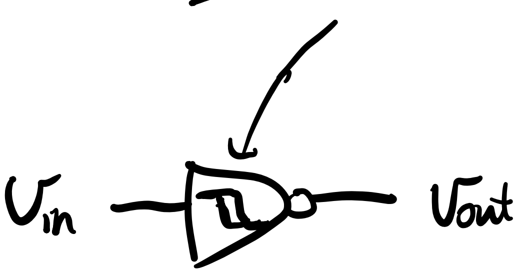
2. Binary Numbers.

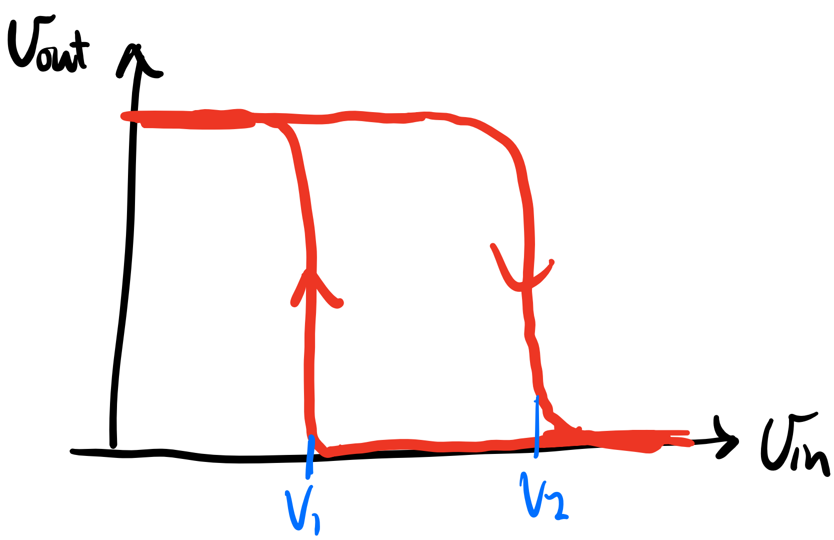
Day 1 of ADC:

- build and test:
  1. Clock generater
  2. Reset Pulse Generator
  3. Flip-Flop.
  4. Counter (pair of ÷10)

Analysis of circuits ① & ②.

Inverters that we use in the lab have hysteresis.

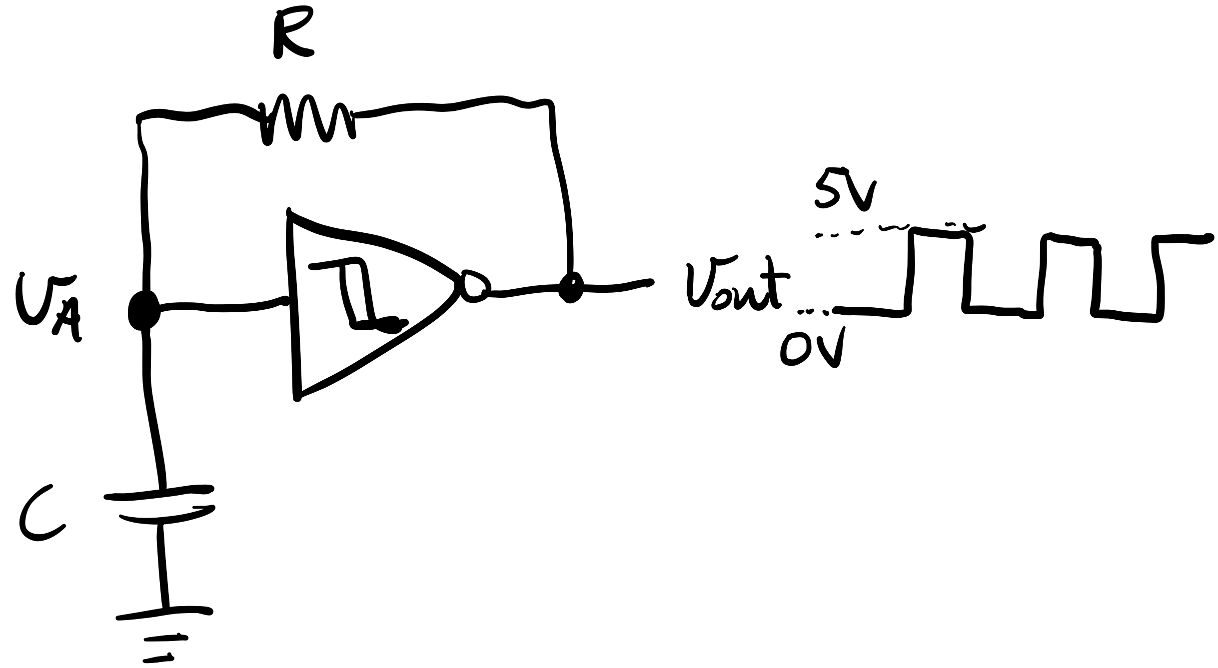




Hysteresis implies that the H→L & L→H transistions occur at different values of V_{in}. This property is important for circuits ① & ②.

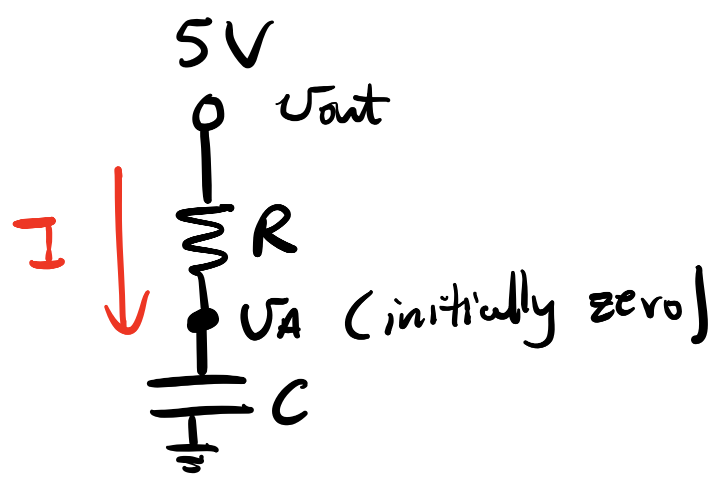
Square-Wave Generator.

No input volt. supplied to this circuit. We can meas. volt. V_A at input of inverter using an osc.

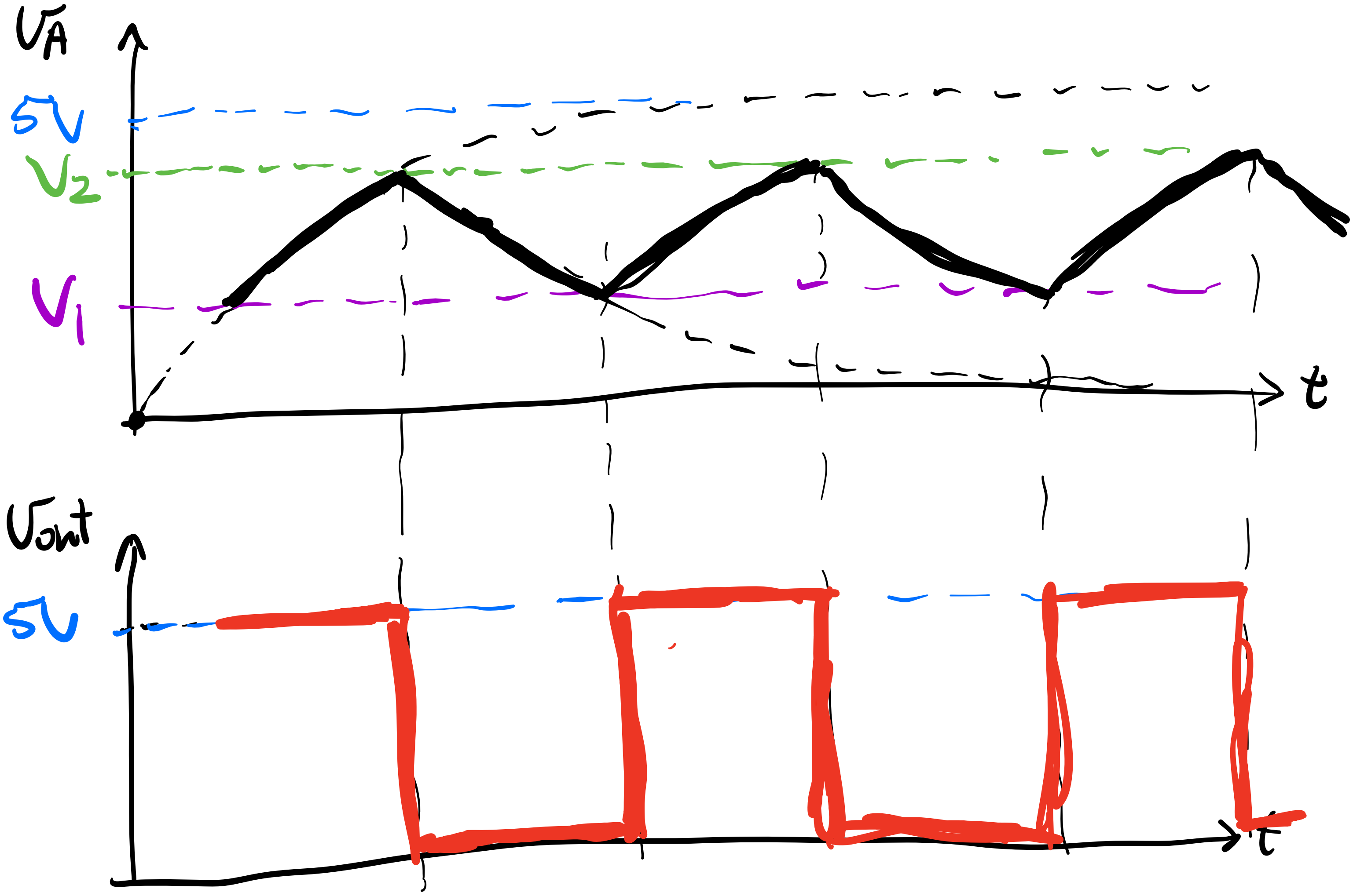


Assume that initially V_A is LO & V_{out} is HI.

Equivalent circuit, in this case is:

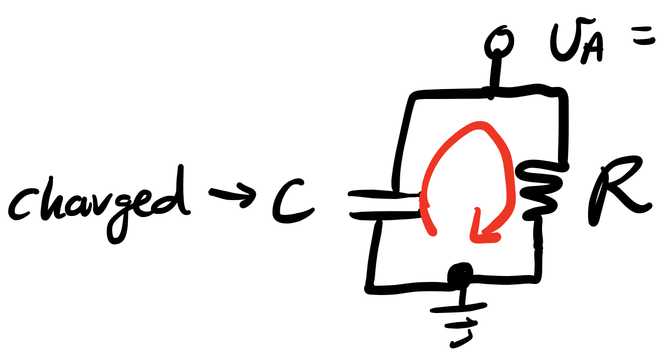


Initially, capacitor is uncharged. However, as time evolves, the cap. will charge b/c of current through R.



Assume now that V_A is HI & V_{out} is LO.

Equivalent circuit for this case is:



cap. starts to discharge through resistor R.

Capacitor discharges until V_A reaches V_1 at which pt., the out transitions from LO → HI.

Repeated charging & discharging of the capacitor causes the output of the inverter to osc. between HI & LO states → sq. wave osc.

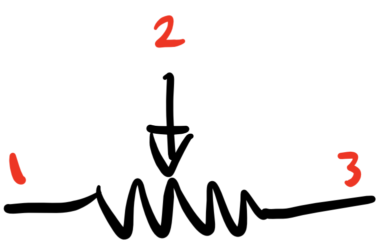
The period of the osc. is determined by the RC charging/discharging time constant.

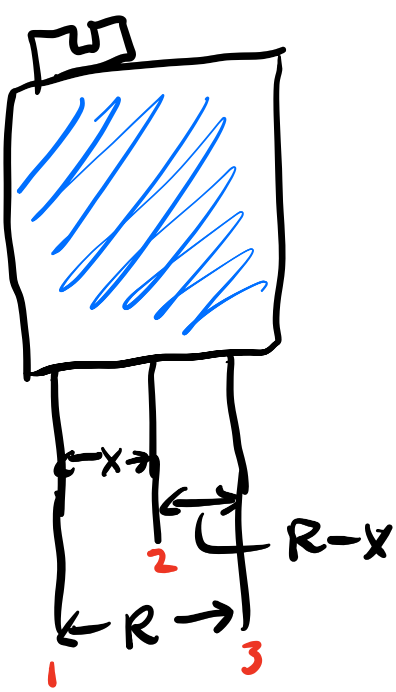
Circuit ① includes a variable resistor which allows us to tune the period of our sq. wave output.

- Resistance across outer two leads is const. $R = 10k\Omega$
- Resistance between left & centre leads is x, where

$$0 < x < 10k\Omega.$$

circuit symbol

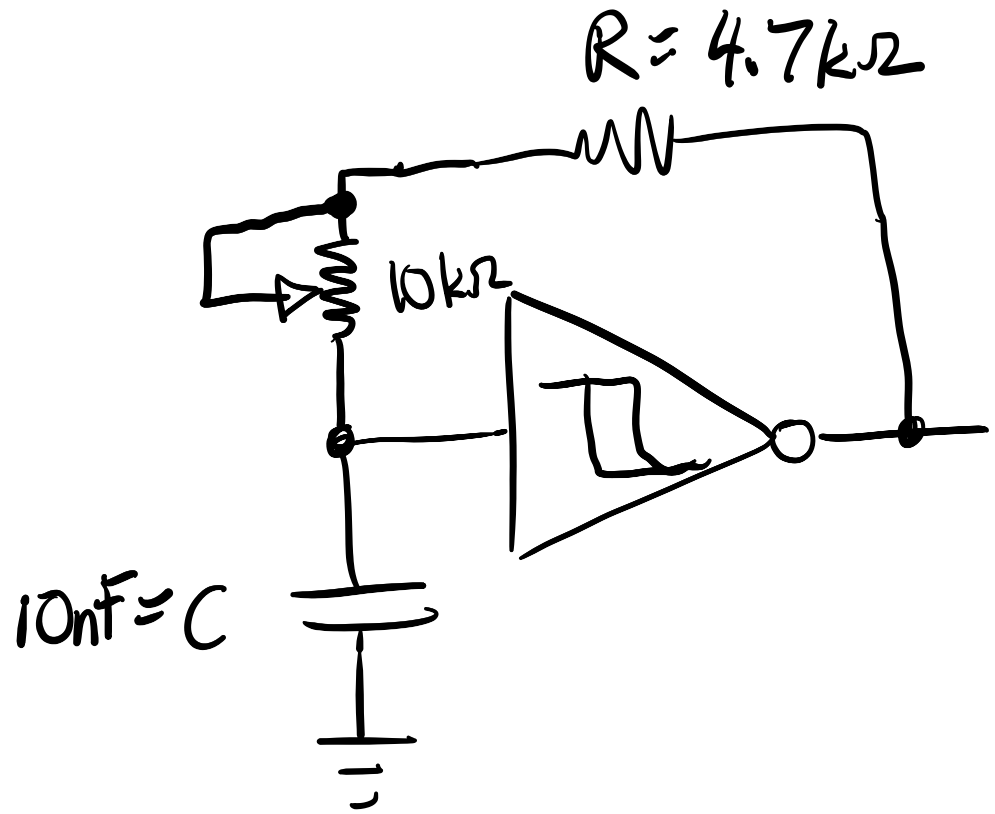




Change the value of x using screw at top.

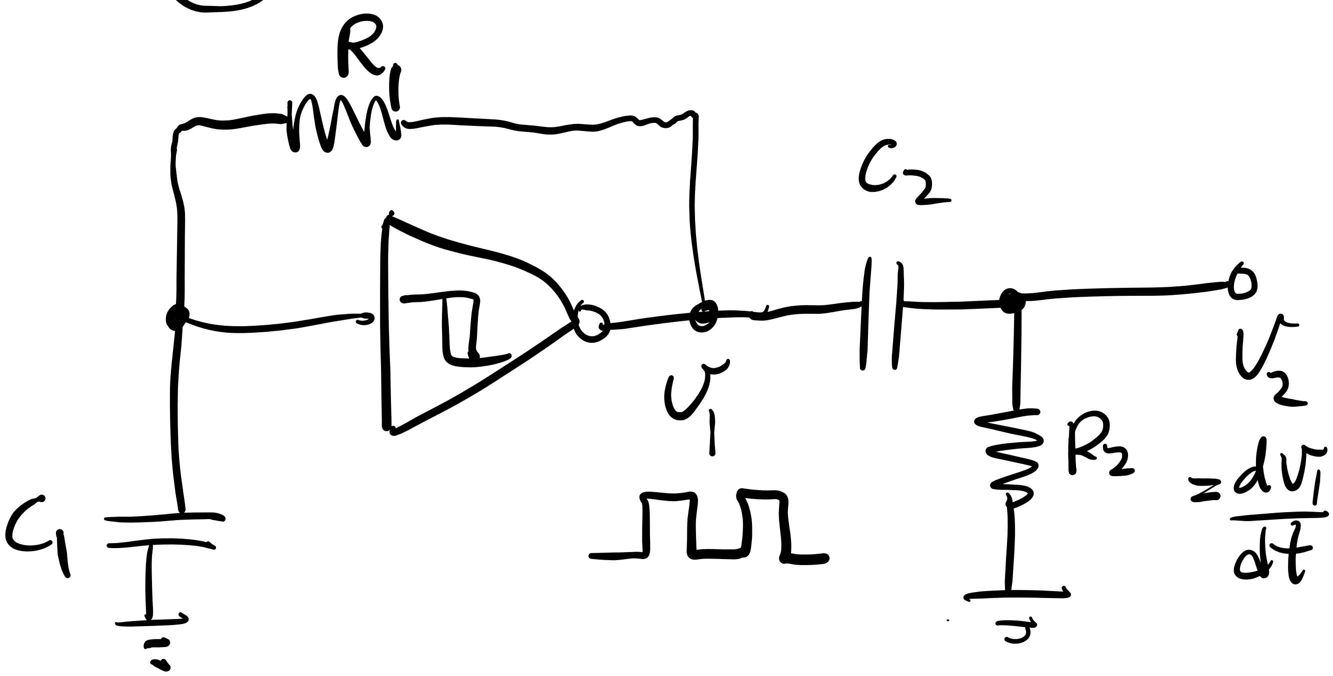
Between the right & centre leads, the resistance is R−x $(0 < R-x < 10\,k\Omega)$

Circuit ①

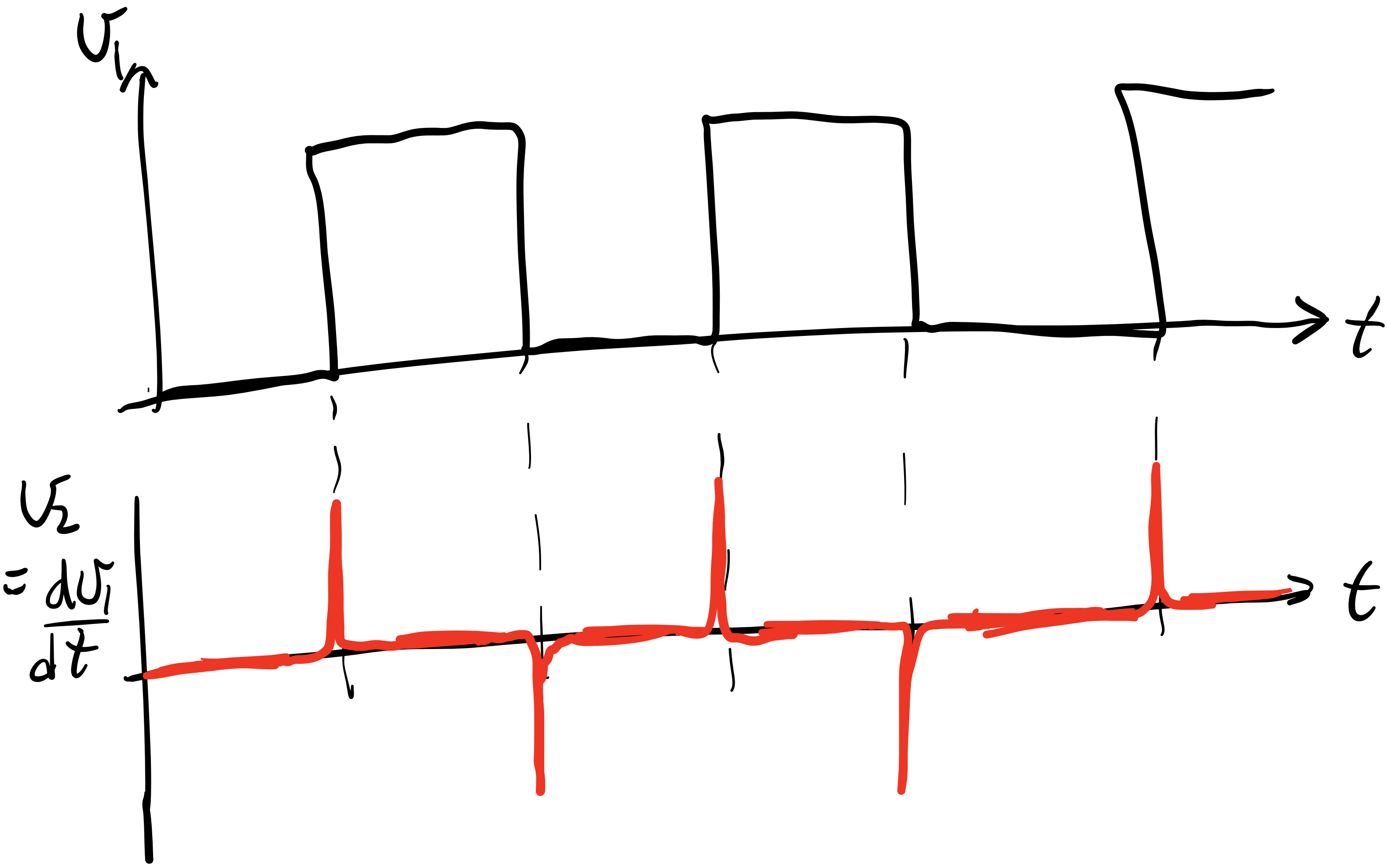


Now total resistance in feedback loop is R + x (assuming we've short circuited the R−x resistance).

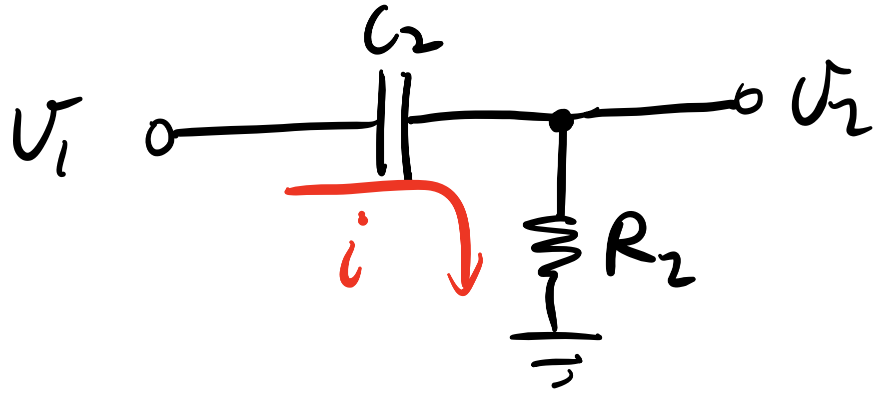
Circuit ②



If $v_2 = \frac{dv_1}{dt}$, then:



Consider



$$V_1 - V_{C_2} = V_2$$

know $C_2 = \frac{q}{V_{C_2}}$

$\therefore$ $V_{C_2} = \frac{q}{C_2}$

$$\therefore \quad V_{C_2} = V_1 - V_2$$

$$\therefore \quad q = C_2(V_1 - V_2)$$

approximation: assume $V_1 \gg V_2$

If this assumption is valid, then

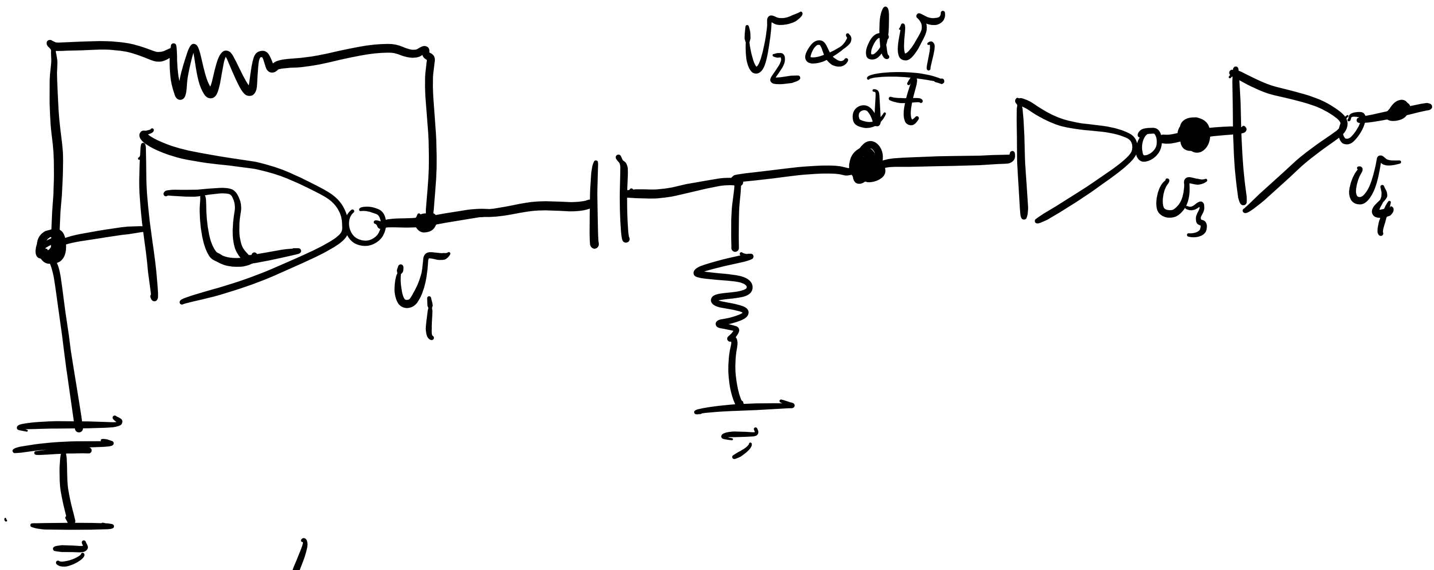
$$q \approx C_2 V_1$$

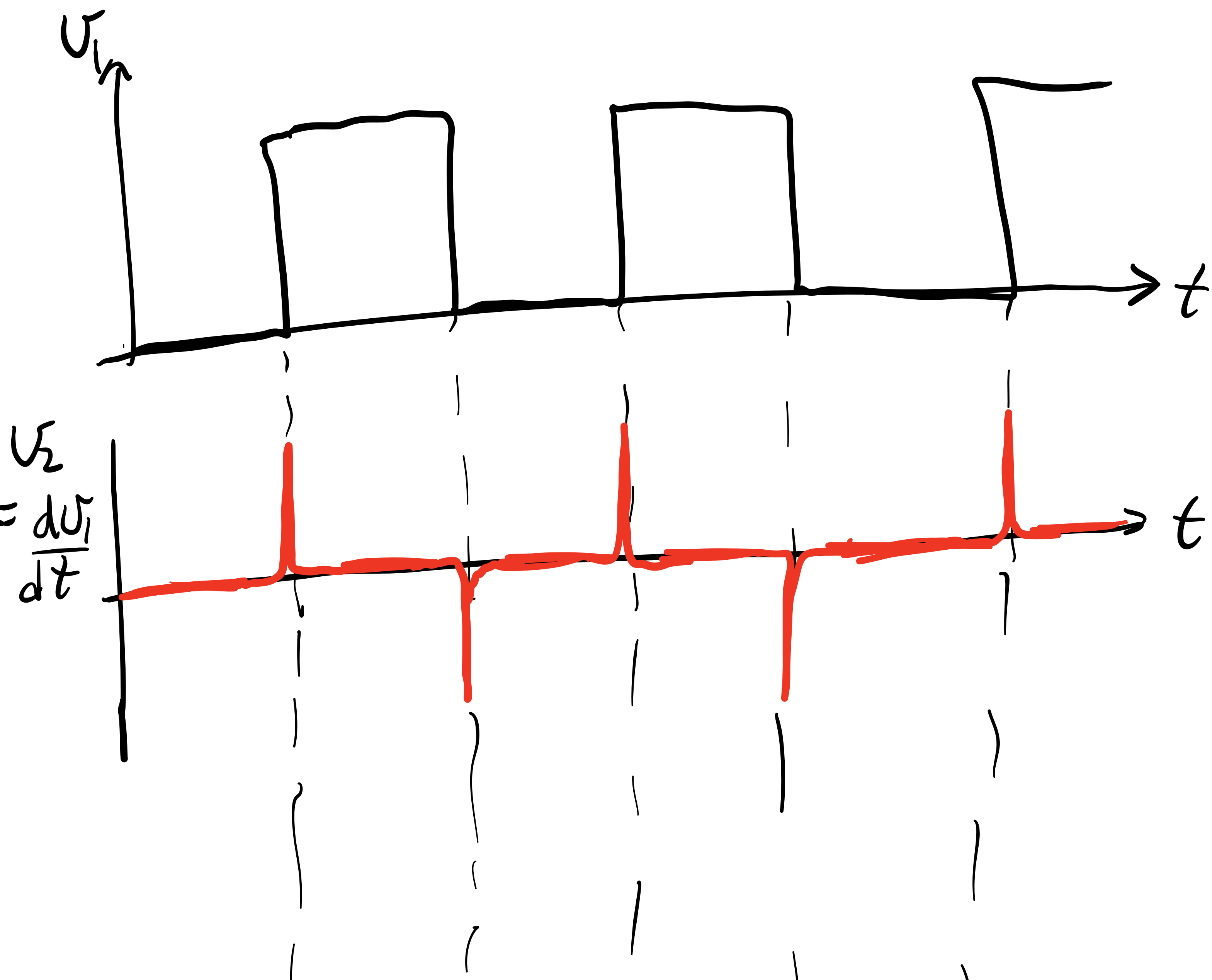
$$\therefore \quad i = \frac{dq}{dt} \approx C_2 \frac{dV_1}{dt}$$

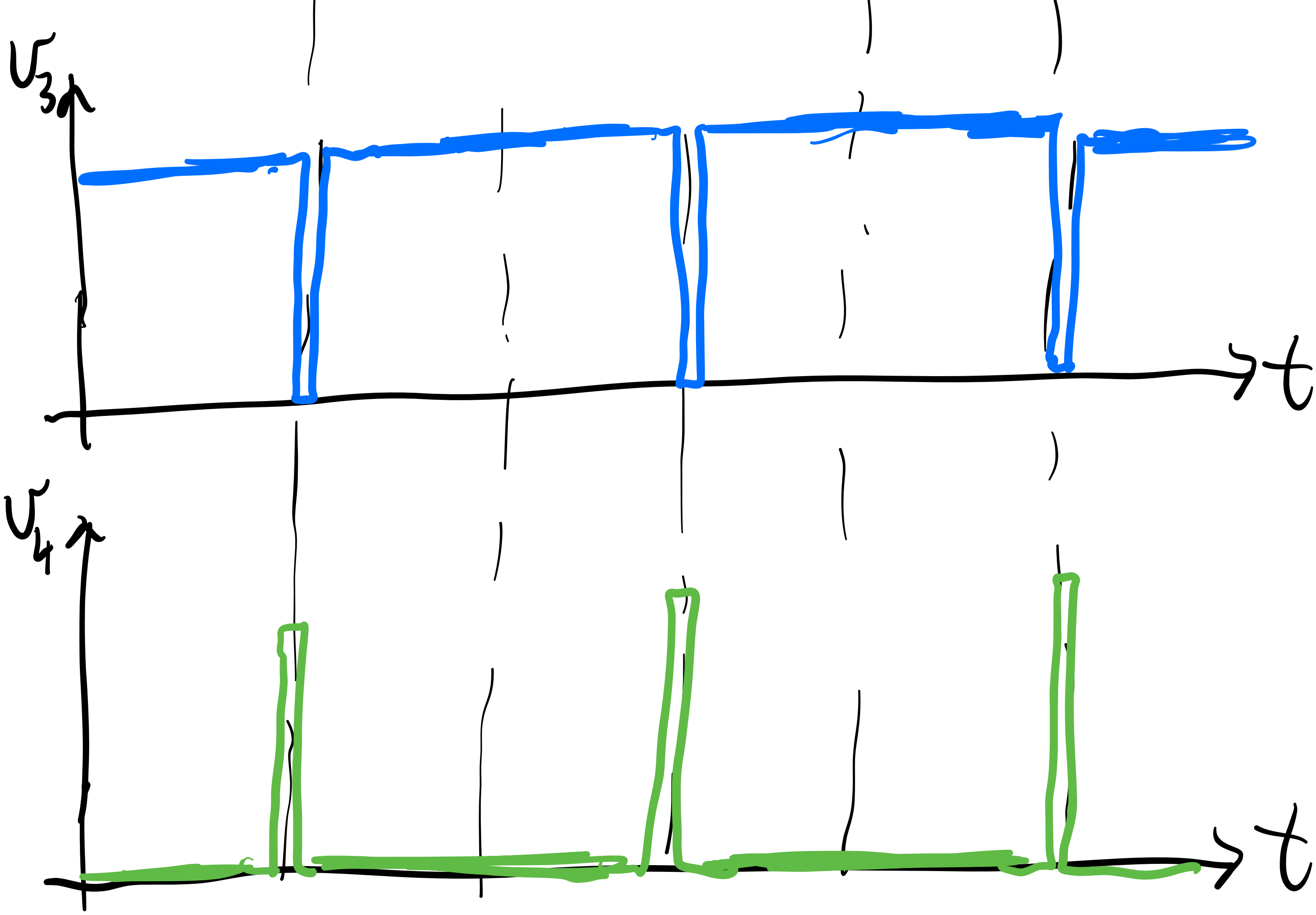
since $V_2 = iR_2$,

$$\boxed{V_2 = R_2 C_2 \frac{dV_1}{dt}}$$

Complete circuit ②.







v_3
t
v_4
t